

DLC Display Co., Limited

德爾西顯示器有限公司



MODEL No: DLC320160CFWG

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Record of Revision

Date	Revision No.	Summary
2016-07-01	1.0	Rev 1.0 was issued
2020-12-07	2.0	Improve drawing information and modify operating voltage

1. Scope

This data sheet is to introduce the specification of DLC320160CFWG, FSTN module. It is composed of a LCD panel, driver IC, FPC and backlight unit.

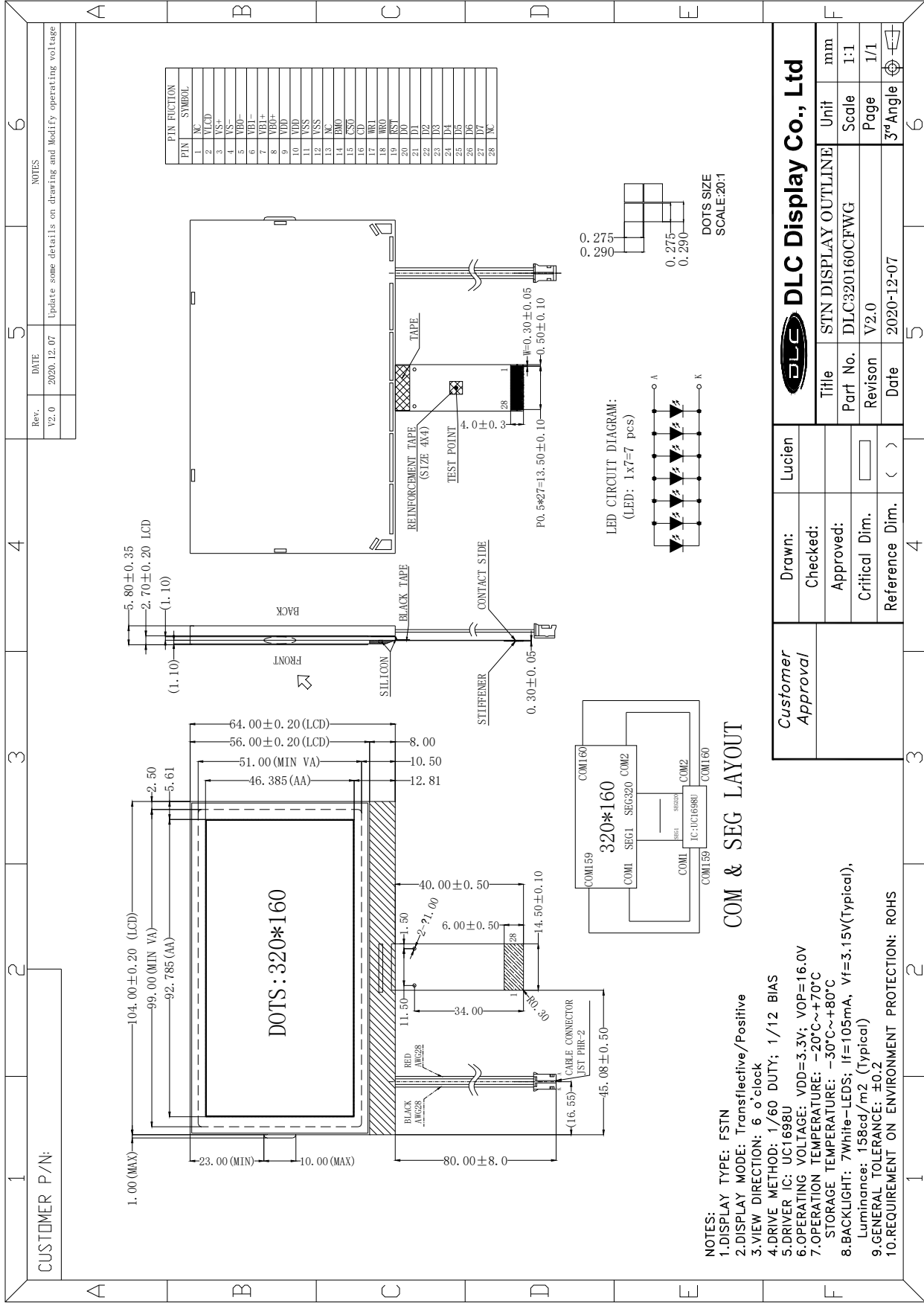
2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

3. General Information

Item	Contents	Unit
LCD Type	FSTN	
Polarizer Type	Transflective / Positive	
Viewing Direction	6 o'clock	
Interface	8-bits CPU	
Number of Dots	320 x 160	dot
Dot size (W×H)	0.275 x 0.275	mm
Dot pitch (W×H)	0.290 x 0.290	
Active Area	92.785 (W) x 46.385 (H)	mm
Outline Dimension (W x H x D)	104(W) x 64(H) x 5.8(T)max	mm
LCD Controller & Driver	UC1698U	
LCD Driving Method	1/160 Duty ,1/12 Bias	
Backlight Type	LED	
Backlight Color	White	
Operating Temperature	-20℃ ~ +70℃	
Storage Temperature	-30℃ ~ +80℃	
Weight	Approx: 39.0	g

4. Outline Drawing



DLC Display Co., Ltd	
Drawn: Lucien	Unit: mm
Checked:	Scale: 1:1
Approved:	Page: 1/1
Critical Dim.:	3° Angle
Reference Dim.:	
Title: STN DISPLAY OUTLINE	Part No. DLC320160CFWG
Revision: V2.0	Date: 2020-12-07

5. Interface signals

Pin No.	Symbol	Description
1	NC	No connection.
2	VLCD	High voltage LCD Power Supply.
3	VS+	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX-, and a capacitor of CS value between VS+ and VS-.
4	VS-	
5	VB0-	
6	VB1-	
7	VB1+	
8	VB0+	
9	VDD	Power supply for logic (+3.3V).
10	VDD	
11	VSS	Ground (0V).
12	VSS	
13	NC	No connection.
14	BM0	Bus mode : [0]8080/8-bit, [1]6800/8-bit
15	$\overline{CS0}$	Chip Select.
16	CD	Selects Control data or Display data for read/write operation. "L": Control data "H": Display data.
17	WR1	WR [1:0] control the read/write operation of the host interface. See section Host Interface for more detail. In the 8080 mode WR1 control the read operation and is LOW-active. In the 8080 mode WR0 control the write operation and is LOW-active.
18	WR0	
19	\overline{RST}	When $\overline{RST}="L"$, all control registers are re-initialized by their default states. Since UC1698u has built-in Power-ON reset and software reset commands, \overline{RST} pin is not required for proper chip operation.
20	D1	Bi-directional bus for parallel host interfaces.
21	D1	
22	D2	
23	D3	
24	D4	
25	D5	
26	D6	
27	D7	
28	NC	No connection.

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD	-0.3	+4.0	V	
LCD Driving Voltage	VLCD	-0.3	+19.8	V	
Digital input signal	Vin	-0.4	VDD+0.5	V	

Note 1: The module may be destroyed if they are used beyond the absolute maximum rating.

Note 2 :All voltage values are referenced to VSS= 0 V.

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	°C	
Storage Temperature	TSTG	-30	80	°C	

7. Electrical Specifications

7.1 Electrical characteristics

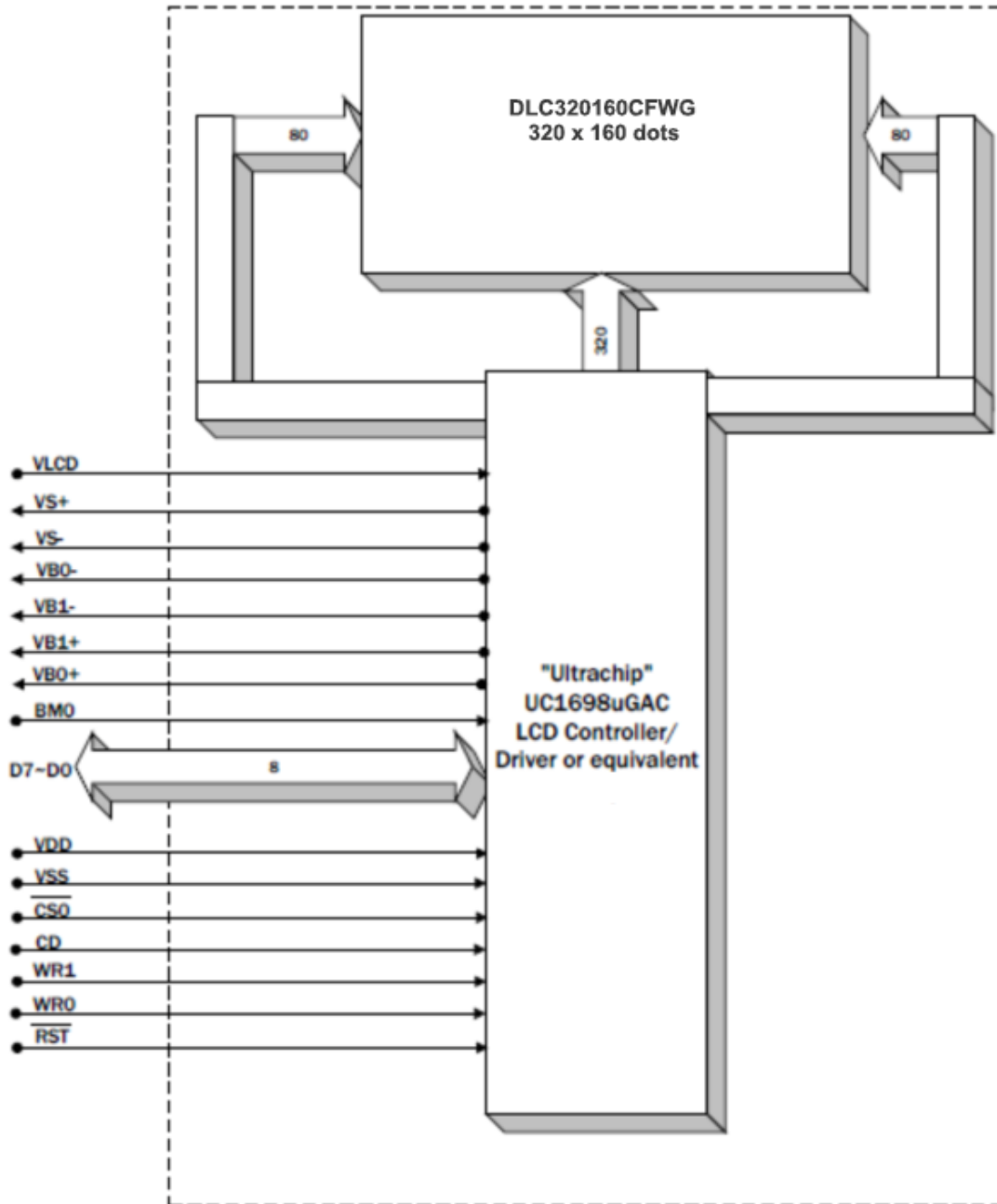
Ta=25°C, VDD=3.3±0.165V, Vss=0V

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage (Logic)	VDD-VSS		3.135	3.3	3.465	V
Supply voltage (LCD) (Built-in)	VLCD-VSS	Ta = -20°C VDD=+3.3V,Note1	-	16.9	-	V
		Ta = +25°C VDD=+3.3V,Note1	15.7	16.0	16.9	V
		Ta = +70°C VDD=+3.3V,Note1	-	15.6	-	V
Input High Voltage	V _{IH}		0.8*VDD	-	-	V
Input Low Voltage	V _{IL}		-	-	0.2*VDD	V
Supply Current (Logic & LCD)	IDD	Character mode VDD=+3.3V, Note1	-	1.6	3.2	mA
		Checkerboard mode VDD=+3.3V, Note1	-	1.6	3.2	mA

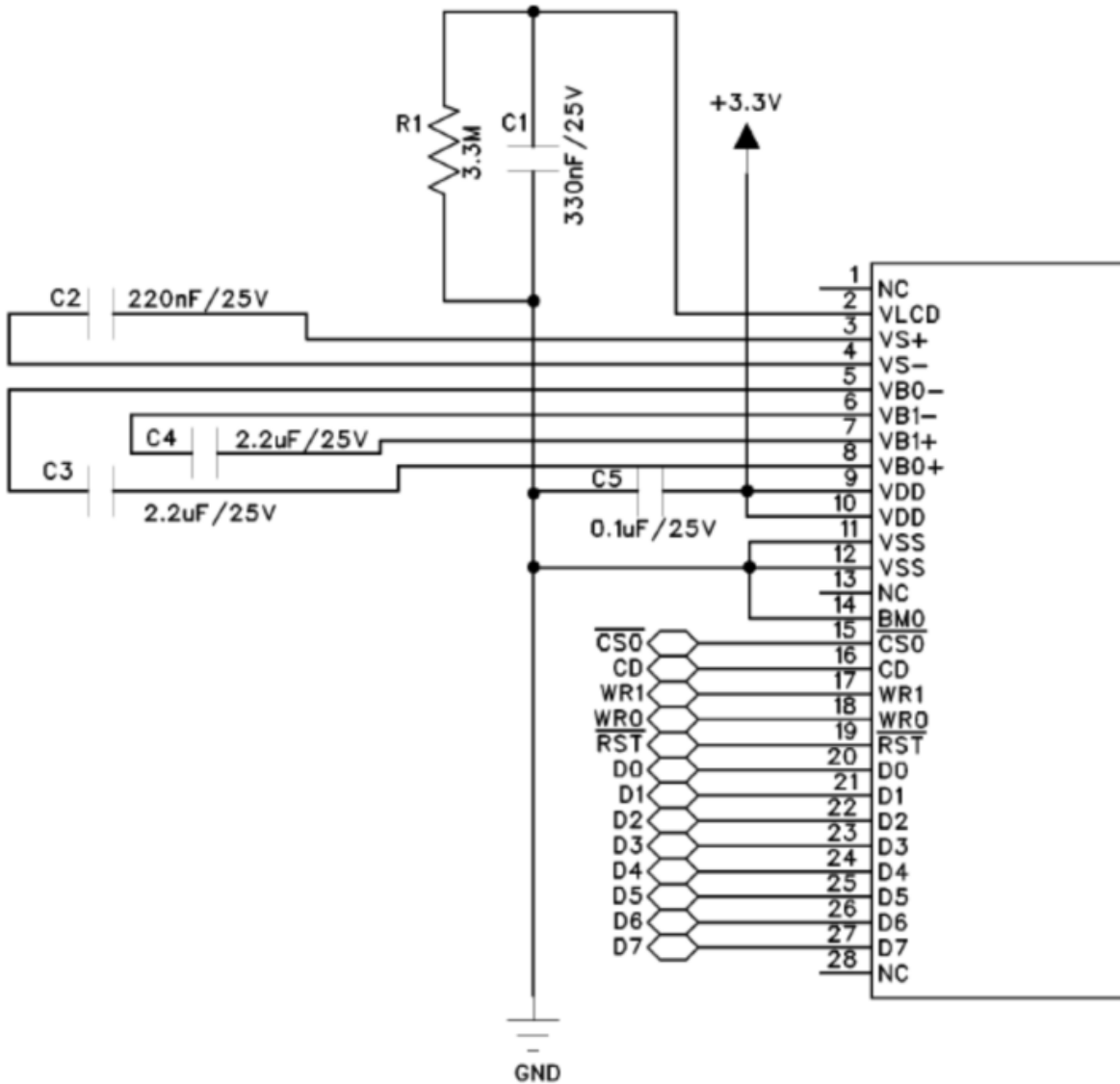
Note 1 : There is tolerance in optimum LCD driving voltage during production. Minimum and maximum LCD driving voltages indicate the range of optimum LCD driving voltage shift due to production tolerance. Please adjust LCD driving voltage manually to obtain the best module performance.

Note 2 : Do not display a fixed pattern for more than 30 minutes. Because it may cause image sticking due to LCD characteristics. It is recommended to change display pattern frequently . If customer must fix display pattern on the screen, Please consider to activate screen saver.

7.2 Block Diagram



7.3 Application Circuit (for reference only)



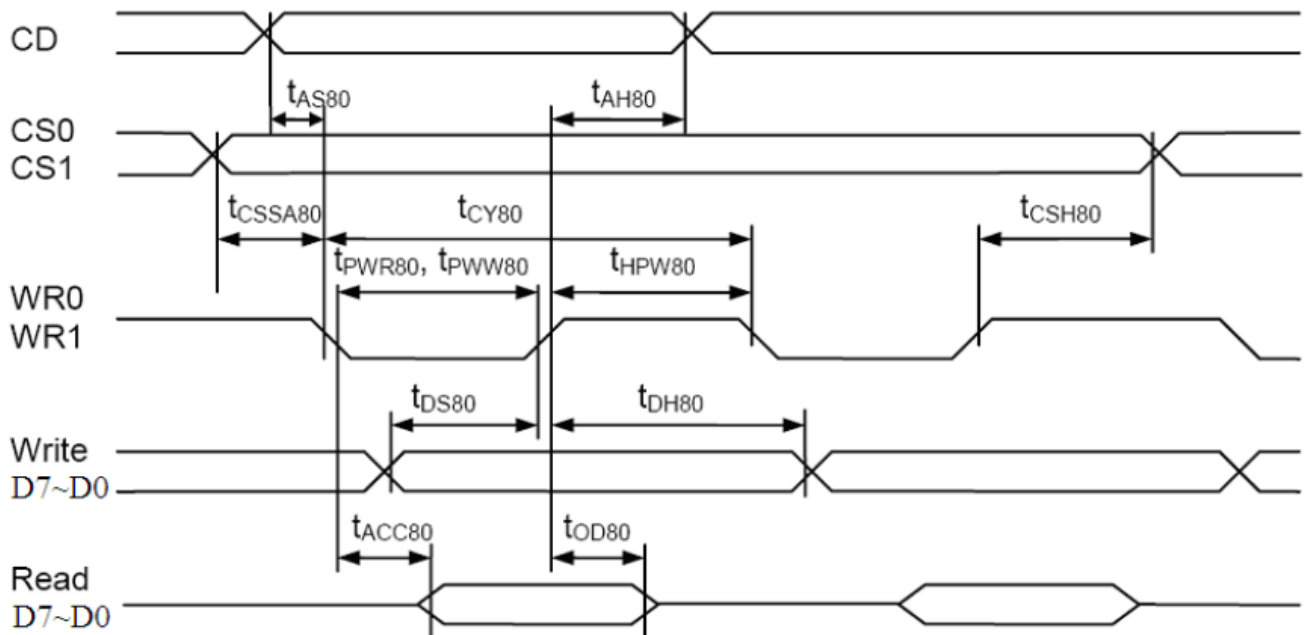
8. Timing Specification

8.1 Parallel Bus Timing Characteristics (for 8080 MCU)

At $T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 3.3 \pm 0.165\text{V}$, $V_{SS} = 0\text{V}$

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	-	nS
t_{CY80}		System cycle time	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	200 / 160 130 / 110 / 120	-	nS
t_{PWR80} / t_{PWW80}	WR1 / WR0	Pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{HPW80}	WR0, WR1	High pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{DS80} t_{DH80}	D7~D0	Data setup time Data hold time		30 10	-	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	$C_L = 100\text{pF}$	- 15	80 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 15		nS

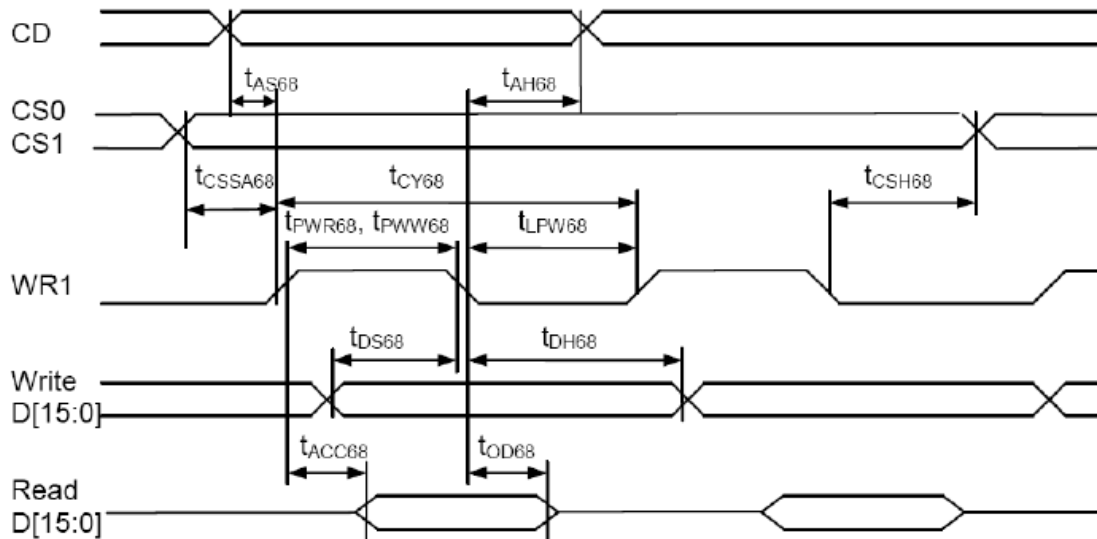
Note: The rising time and the falling time are stipulated to be equal to or less than 15nS.



8.2 Parallel Bus Timing Characteristics (for 6800MCU)

At Ta=-20°C to +70°C, VDD=3.3±0.165V, Vss=0V

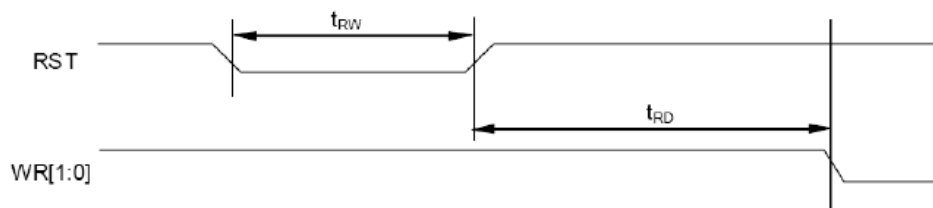
Symbol	Signal	Description	Condition	Min.	Max.	Unit
(Read / Write)						
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	-	nS
t_{CY68}		System cycle time	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	200 / 160 130 / 110 / 120	-	nS
t_{PWR68} / t_{PWW68}	WR1	Pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{LPW68}		Low pulse width	16-bit bus 8-bit bus LC[7:6]=10b LC[7:6]=01b	85 / 65 50 / 40 / 45	-	nS
t_{DS68} t_{DH68}	D15~D0	Data setup time Data hold time		30 10	-	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	$C_L = 100pF$	- 15	80 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 15		nS



8.3 Reset Input Timing

At Ta=-20°C to +70°C, VDD=3.3±0.165V, Vss=0V

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	-	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	-	mS



8.4 Command Table

The following is a list of host commands supported by UC1698u

[C/D] : 0: Control, 1: Data

[W/R] : 0: Write Cycle, 1: Read Cycle

[D7-D0] : #: Useful Data bits -: Don't Care

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A	
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A	
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	Product Code: 8h	
				Ver	PMO[6:0]						Product Code			PID[1:0]
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0	
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0	
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0	
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b	
7	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A	
		0	0	#	#	#	#	#	#	#	#			
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0	
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0	
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0	
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0	
10	Set V _{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H	
		0	0	#	#	#	#	#	#	#	#			
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0	
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b	
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0	
		0	0	#	#	#	#	#	#	#	#			
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b	
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0	
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0	
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b	
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0	
19	Set N-Line Inversion	0	0	-	-	-	#	#	#	#	#	Set NIV[4:0]	1DH	
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)	
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b	
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b	
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A	
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A	
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A	
		0	0	#	#	#	#	#	#	#	#			
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12	
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0	
		0	0	-	#	#	#	#	#	#	#			
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159	
		0	0	-	#	#	#	#	#	#	#			
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		Set WPP0	0
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Shared with MTP commands	Set WPC1	127
		0	0	#	#	#	#	#	#	#	#		Set WPP1	159
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Shared with MTP commands	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		Set WPP1	159
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Shared with MTP commands	Set WPC1	127
		0	0	#	#	#	#	#	#	#	#		Set WPP1	159
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside	
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H	
		0	0	-	-	-	#	#	#	#	#			

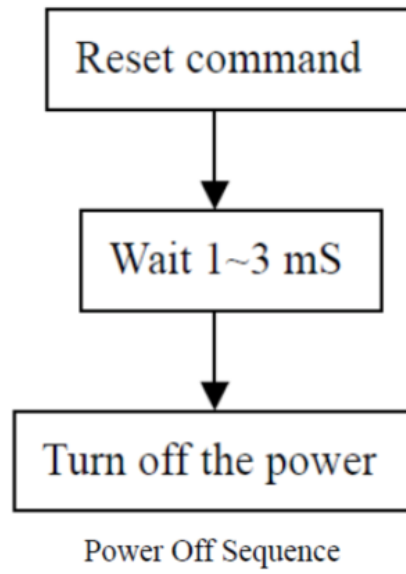
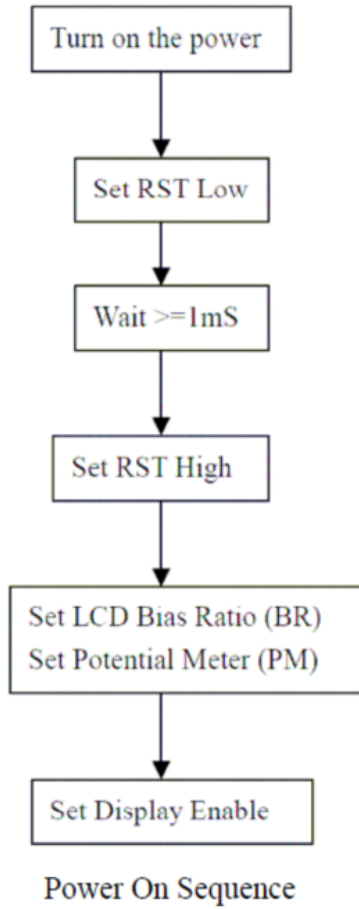
#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
36	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[6:0] MTPM1[1:0]	0	
		0	0	-	#	#	#	#	#	#	#			
		0	0	-	-	-	-	-	-	-	#			#
37	Set V _{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program commands	Set MTP1	N/A
38	Set V _{MTP2} Potentiometer	0	0	#	#	#	#	#	#	#	#		Set MTP2	N/A
		0	0	1	1	1	1	0	1	0	1		Set MTP3	N/A
39	Set MTP Write Timer	0	0	#	#	#	#	#	#	#	#		Set MTP4	N/A
40	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1	Set MTP4	N/A	
		0	0	#	#	#	#	#	#	#	#			

8.5 Initial Code Setting (for reference only)



Command	Value
Set Column Address LSB	0x00
Set Column Address MSB	0x10
Set Temp Compensation	0x24
Set Power Control	0x2B
Set Row Address LSB	0x60
Set Row Address MSB	0x70
Set Vbias Potentiometer	0x81 0x3C
Set Partial Display Control	0x84
Set RAM Address Control	0x89
Set Fixed Lines	0x90 0x00
Set Line Rate	0xA2
Set All-Pixel-On	0xA4
Set Inverse Display	0xA6
Set Display Enable	0xAD
Set LCD Mapping control	0xC4
Set N-line Inversion	0xC8 0x0F
Set Color Pattern	0xD1
Set Color Mode	0xD6
Set COM Scan Function	0xD8
System Reset	0xE2
Set LCD Bias Ratio	0xEB
Set COM End	0xF1 0x9F
Set Partial Display Start	0xF2 0x00
Set Partial Display End	0xF3 0x9F

8.6 Power on/ off sequence



9. Optical Specification

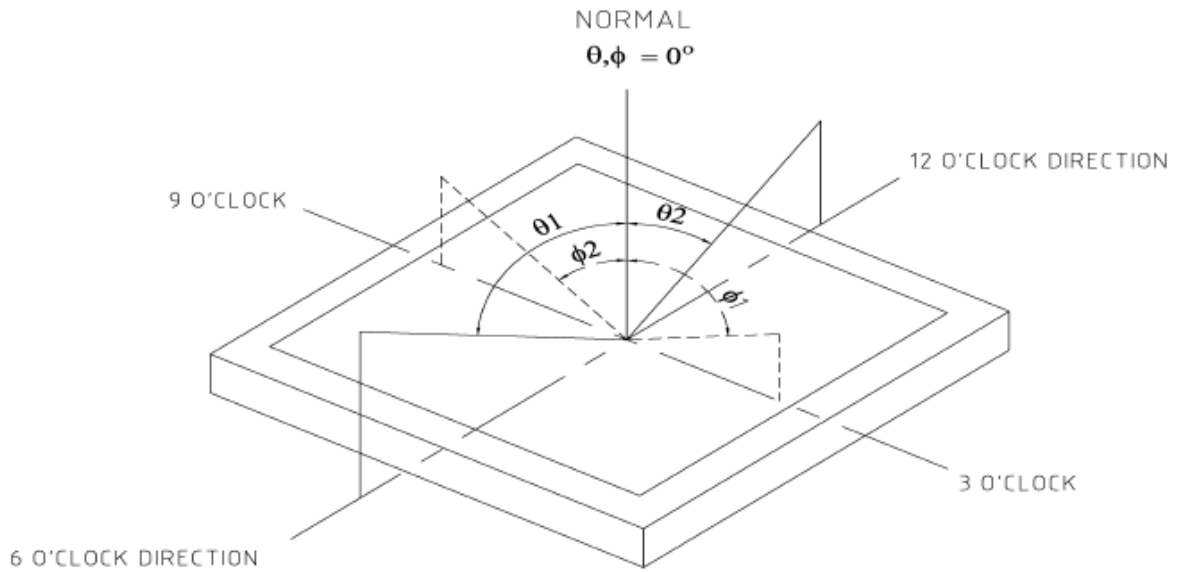
Item	Symbol	Temp. °C	Value			Unit	Condition	
			Min.	Typ.	Max.			
Driving voltage	Vop (VLCD-VSS)	-20	-	16.9	-	V	Vop= optimum voltage (Remark 1)	
		+25	15.7	16.3	16.9			
		+70	-	15.6	-			
Response time	Ton	-20	-	855	1280	msec	Vop= Optimum voltage $\theta = 0^\circ, \phi = 0^\circ$	
	Toff		-	5840	8760			
	Ton	+25	-	175	228			
	Toff		-	235	305			
	Ton	+70	-	150	195			
	Toff		-	240	315			
Optimum viewing area Cr ≥ TBD	θ1(6 o'clock)	+25	40	50	-	DEG	φ = 0°	Vop= Optimum voltage (Remark 2)
	θ2(12 o'clock)		40	50	-			
	φ1(3 o'clock)		35	45	-		θ = 0°	
	φ2(9 o'clock)		35	45	-			
Contrast ratio	Cr	+25	3.0	5.0	-	-	Vop = Optimum voltage $\theta = 0^\circ, \phi = 0^\circ$	

Remark 1: There is tolerance in optimum LCD driving voltage during production. Minimum and maximum LCD driving voltages indicate the range of optimum LCD driving voltage shift due to production tolerance. Please adjust LCD driving voltage manually to obtain the best module performance.

Remark 2: Due to hardware limitation, the maximum measurable angle is 50°.

9.1 Optical Characteristics Definition

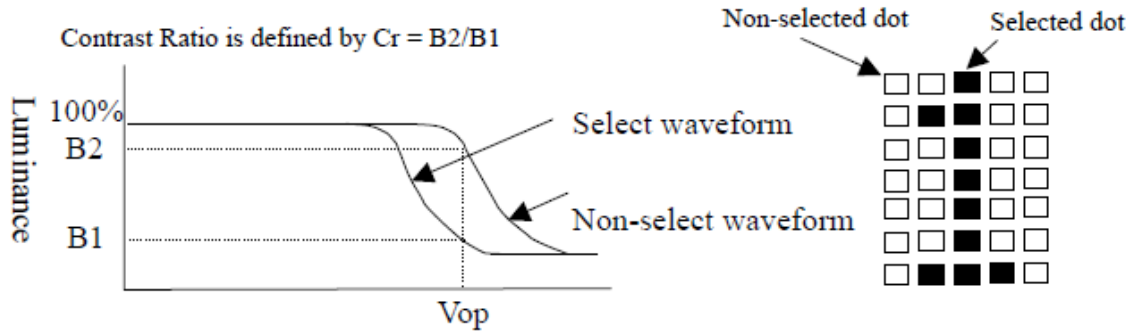
a.) Viewing Angle



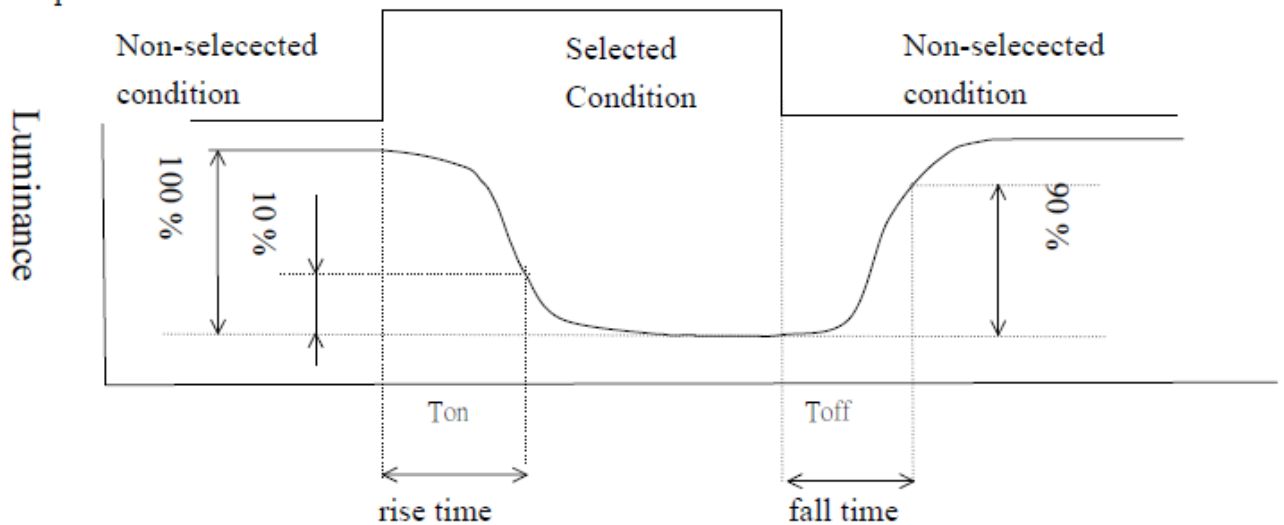
b.) Contrast Ratio

B1 = segments luminance in case of non-selected waveform

B2 = segments luminance in case of selected waveform



c.) Response Time



10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70°C, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20°C, 120hrs	Per table in below
3	High Temp Storage	Ta=+80°C, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30°C, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40°C, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30°C 30 min~+80°C 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω , 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11 . Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

- A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
- C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- D. Provide a space so that the panel does not come into contact with other components.
- E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
- G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
- H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

- A. Ground soldering iron tips, tools and testers when they are in operation.
- B. Ground your body when handling the products.
- C. Power on the LCD module before applying the voltage to the input terminals.
- D. Do not apply voltage which exceeds the absolute maximum rating.
- E. Store the products in an anti-electrostatic bag or container.

11.4 Storage

- A. Store the products in a dark place at $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

- A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

